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... For example, in **Verilog** [12, 18], data types are ... we have developed extensions to **VHDL** to improve ... that information is transferred using the **send** and **receive** ...

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... Expert Douglas HDL Instructor (**Verilog-VHDL**) info@ALSE ... Standard & 100% portable **VHDL** Description : - Synthesis ... type State_Type is (Idle, Get, **Send**); signal State ...

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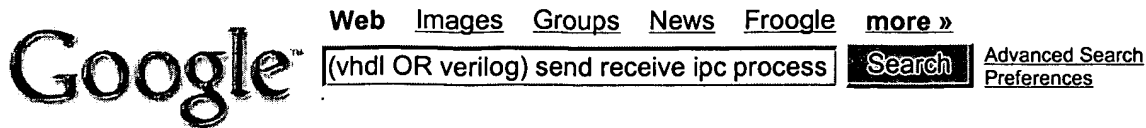
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... deterministic For example when a **process receive** at the ... passing processes communicatethrough
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... .. init A; **send** A(x); ... init A; **receive** A(y ... vpp .vhdl .vhdl Design file Internal
 representation generator Parsing .vhdl .vhdl .vhdl INPUT: OUTPUT ...
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... Unit integrated as an IP-block at the **VHDL**-level ... terminate, etc), inter-**process** com-
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... that performs technology mapping of RT-code (described in **VHDL** or **Verilog**). ... Condition
 Message Token Based Blocking **Receive** Non Blocking **Send** Data Deadlock ...

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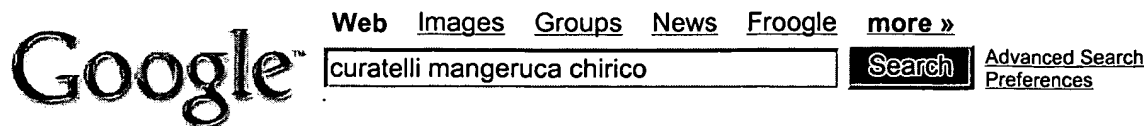
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